In the Claims

1. (Currently Amended) A method comprising:

providing a semiconductor substrate that includes a memory container including a double-sided capacitor; and

vapor phase etching a layer adjacent to [[the]] a side wall of the memory container with a vapor including a surface tension lowering agent.

2. (Previously Presented) The method of claim 1, wherein the vapor phase etching comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor including a carboxylic.

3. (Canceled)

4. (Previously Presented) The method of claim 1, wherein the vapor phase etching comprises vapor phase etching an oxide layer adjacent to the side wall of the memory container.

5. (Previously Presented) The method of claim 1, wherein the vapor phase etching comprises vapor phase etching a borophosphosilicate glass (BPSG) material adjacent to the side wall of the memory container.

6. (Previously Presented) The method of claim 1, wherein the vapor phase etching comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor including hydrogen fluoride and an etch initiator composition.

7. (Previously Presented) A method comprising:

providing a semiconductor substrate that includes a double-sided capacitor memory container; and

etching a layer adjacent to a side wall of the double-sided capacitor memory container with vapor comprising vapor for reducing surface tension that includes methanol.

8. (Previously Presented) The method of claim 7, wherein the etching comprises etching an insulator layer adjacent to the side wall of the double-sided capacitor memory container with the vapor comprising vapor for reducing surface tension that includes methanol.

9. (Previously Presented) The method of claim 7, wherein the etching comprises etching a doped oxide layer adjacent to the side wall of the double-sided capacitor memory container with the vapor comprising vapor for reducing surface tension that includes methanol.

10. (Previously Presented) The method of claim 7, wherein the etching comprises etching an insulator layer adjacent to the side wall of the double-sided capacitor memory container with the vapor comprising vapor for reducing surface tension that includes hydrogen fluoride.

11. (Previously Presented) A method of fabricating a semiconductor circuit element, the method comprising:

placing a semiconductor substrate that includes a double-sided capacitor container in a chamber; and

vapor phase etching a layer adjacent to a side wall of the double-sided capacitor container with a vapor that includes hydrogen fluoride, an etch initiator composition and a surface tension lowering composition that includes an alcohol.

12. (Previously Presented) The method of claim 11, wherein the vapor phase etching comprises vapor phase etching an oxide layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and the surface tension lowering composition that includes alcohol.

13. (Previously Presented) The method of claim 11, wherein the vapor phase etching comprises vapor phase etching an insulator layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and the surface tension lowering composition that includes alcohol.

14. (Previously Presented) The method of claim 11, wherein the vapor phase etching comprises vapor phase etching a layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and the surface tension lowering composition that includes methanol.

15. (Previously Presented) The method of claim 11, wherein the vapor phase etching comprises vapor phase etching a layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, H_2O and the surface tension lowering composition that includes isopropyl alcohol.

16. (Previously Presented) A method of fabricating an integrated circuit, the method comprising:

housing the integrated circuit in a vapor etch chamber; and

vapor phase etching an insulator layer formed adjacent to a double-sided capacitor container in the integrated circuit with a vapor including a surface tension lowering agent, wherein the vapor phase etching of the insulator layer comprises inserting a vapor comprised of a hydrogen fluoride and isopropyl alcohol into the vapor etch chamber.

17. (Original) The method of claim 16, further comprising heating the hydrogen fluoride and the isopropyl alcohol prior to inserting the vapor into the vapor etch chamber.

18. (Previously Presented) The method of claim 16, wherein the vapor phase etching comprises vapor phase etching a doped oxide layer formed adjacent to the double-sided capacitor container in the integrated circuit.

19. (Previously Presented) The method of claim 16, wherein the vapor phase etching comprises vapor phase etching a borophosphosilicate glass (BPSG) layer formed adjacent to the double-sided capacitor container in the integrated circuit.

20. (Previously Presented) The method of claim 16, wherein the inserting the vapor comprises inserting the vapor comprised of hydrogen fluoride, isopropyl alcohol and an etch initiator composition into the vapor etch chamber.

21. (Previously Presented) A method comprising:

placing a substrate that includes an array of memory into a chamber, the array of memory having at least one memory container with a side wall with an embedded capacitor; and

vapor phase etching of a layer of an insulator material formed adjacent to the side wall, wherein the vapor phase etching comprises:

mixing a hydrogen fluoride with a vapor including a surface tension lowering agent including isopropyl alcohol to form a mixed vapor; and

inserting the mixed vapor into the chamber.

22. (Original) The method of claim 21, further comprising heating the hydrogen fluoride and the isopropyl alcohol prior to inserting the mixed vapor into the vapor etch chamber.

23. (Previously Presented) The method of claim 21, wherein the mixing comprises mixing the hydrogen fluoride, the isopropyl alcohol and an etch initiator composition to form the mixed vapor.

24. (Previously Presented) The method of claim 21, wherein the vapor phase etching comprises vapor phase etching of a layer of oxide formed adjacent to the side wall.

25. (Previously Presented) The method of claim 21, wherein the vapor phase etching comprises vapor phase etching of a layer of silicon dioxide formed adjacent to the side wall.

26. (Previously Presented) A method for fabricating a semiconductor substrate, the method comprising:

placing the semiconductor substrate that includes a memory container into a vapor etching chamber, wherein a side wall of the memory container includes a double-sided capacitor; and

vapor phase etching of a layer of an insulator material formed adjacent to the side wall of the memory container, wherein the vapor phase etching comprises:

mixing an etch initiator composition and surface tension reducing composition including hydrogen fluoride and alcohol to form a mixed vapor;

heating the mixed vapor; and

inserting the mixed vapor into the vapor etching chamber.

27. (Previously Presented) The method of claim 26, wherein the mixing comprises mixing the etch initiator composition and the surface tension reducing composition including hydrogen fluoride and methanol to form the mixed vapor.

28. (Previously Presented) The method of claim 26, wherein the mixing comprises mixing the etch initiator composition and the surface tension reducing composition including hydrogen fluoride and isopropyl alcohol to form the mixed vapor

29. (Previously Presented) The method of claim 26, wherein the vapor phase etching comprises vapor phase etching of a layer of silicon nitride formed adjacent to the side wall of the memory container.

30. (Previously Presented) The method of claim 26, wherein the vapor phase etching comprises vapor phase etching of a layer of silicon oxynitride formed adjacent to the side wall of the memory container.

31. (Original) A method comprising:

placing a semiconductor substrate into a chamber; and

vapor phase etching of an insulator material formed adjacent to a double-sided container on a semiconductor substrate, wherein the vapor phase etching comprises:

forming a vapor that includes an H_2O vapor, an HF gas and a surface tension lowering agent; and

inserting the vapor into the chamber.

32. (Previously Presented) The method of claim 31, wherein the forming comprises forming the vapor that includes H_2O, hydrogen fluoride and carboxylic.

33. (Previously Presented) The method of claim 31, wherein the forming comprises forming the vapor that includes H_2O, hydrogen fluoride and alcohol.

34. (Previously Presented) The method of claim 31, wherein the forming comprises forming the vapor that includes H_2O, hydrogen fluoride and isopropyl alcohol.

35. (Previously Presented) The method of claim 31, wherein the forming comprises forming the vapor that includes H_2O, hydrogen fluoride and methanol.

36. (Previously Presented) The method of claim 31, wherein the vapor phase etching comprises vapor phase etching of a silicon dioxide material formed adjacent to the double-sided container on the semiconductor substrate.

37. (Previously Presented) The method of claim 31, wherein the vapor phase etching comprises vapor phase etching of a doped oxide material formed adjacent to the double-sided container on the semiconductor substrate.

38. (Previously Presented) A method for fabricating a memory array, the method comprising:

forming at least one memory container in a borophosphosilicate glass (BPSG) material on a substrate, wherein a side wall of the at least one memory container includes a double-sided capacitor; and

removing at least a part of the BPSG material based on a vapor wet etch operation with a vapor including a surface tension lowering agent comprising hydrogen fluoride and alcohol.

39. (Previously Presented) The method of claim 38, wherein the removing comprises removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor including a surface tension lowering agent comprising hydrogen fluoride and isopropyl alcohol.

40. (Previously Presented) The method of claim 38, wherein the removing comprises removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor including a surface tension lowering agent comprising hydrogen fluoride and methanol.

41. (Original) A method comprising:

forming at least one memory container in an oxide, wherein a side wall of the at least one memory container includes a double-sided capacitor; and

vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, an etch initiator composition and a surface tension lowering agent.

42. (Previously Presented) The method of claim 41, wherein the forming the at least one memory container comprises forming the at least one memory container in silicon oxide.

43. (Previously Presented) The method of claim 41, wherein the vapor wet etching comprises vapor wet etching with a vapor comprised of hydrogen fluoride, the etch initiator composition and an alcohol.

44. (Previously Presented) The method of claim 41, wherein the vapor wet etching comprises vapor wet etching with a vapor comprised of hydrogen fluoride, the etch initiator composition and isopropyl alcohol.

45. (Previously Presented) The method of claim 41, wherein the vapor wet etching comprises vapor wet etching with a vapor comprised of hydrogen fluoride, the etch initiator composition and methanol.

46-95. (Canceled)